

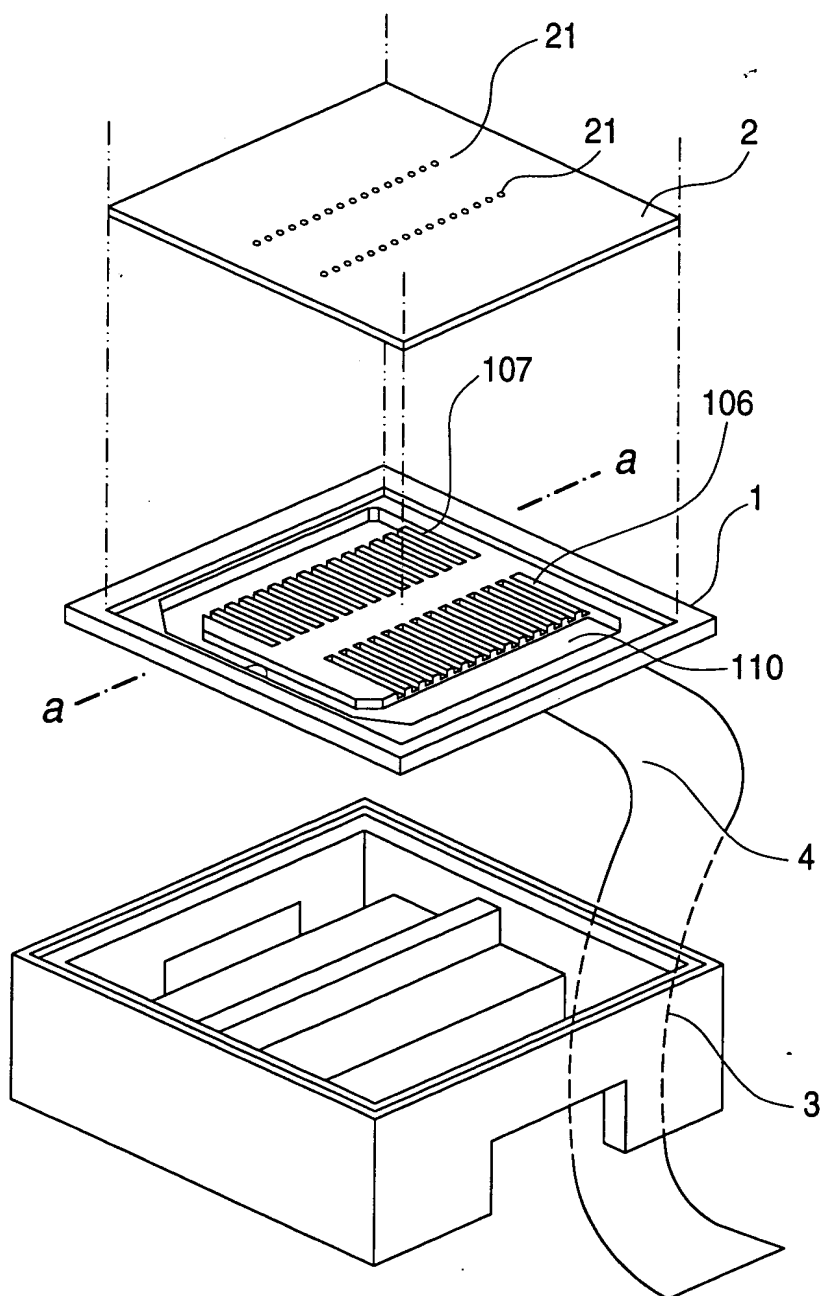
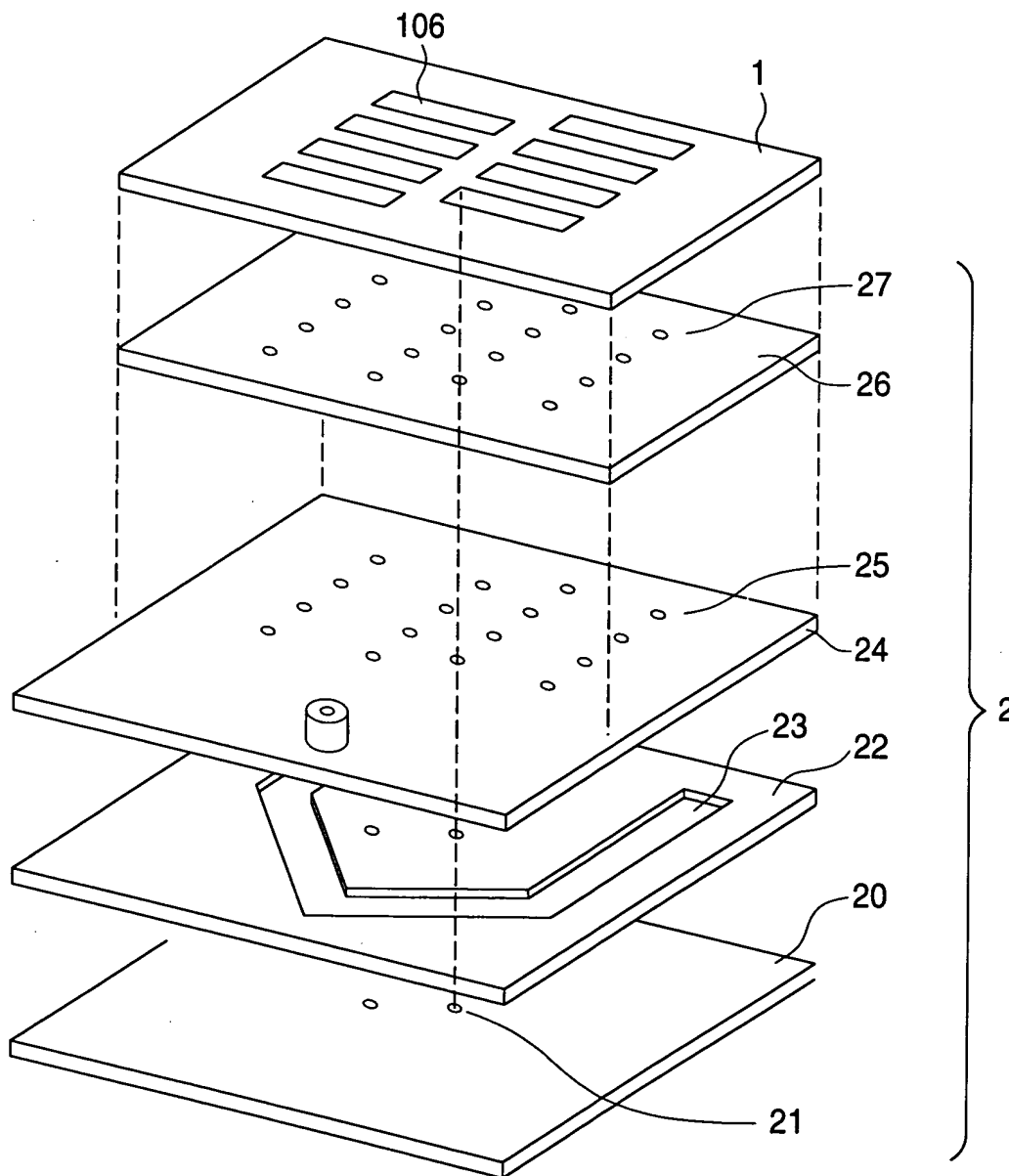
[illegible]

FIG. 2



**FIG. 3**

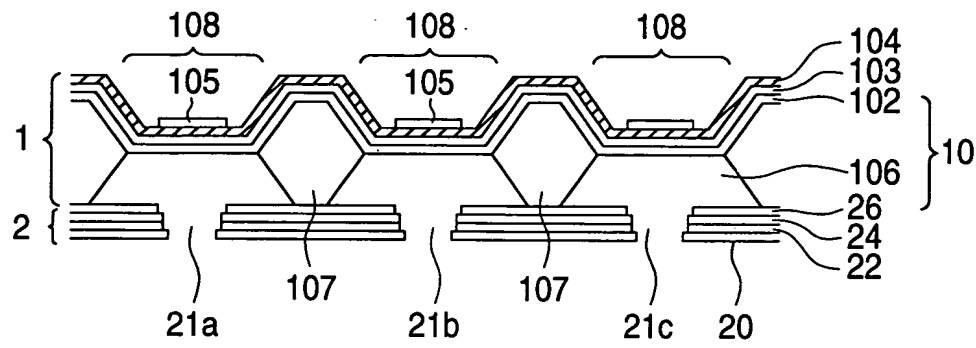


FIG. 4A

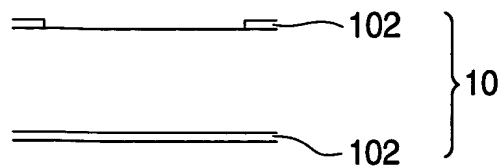


FIG. 4B

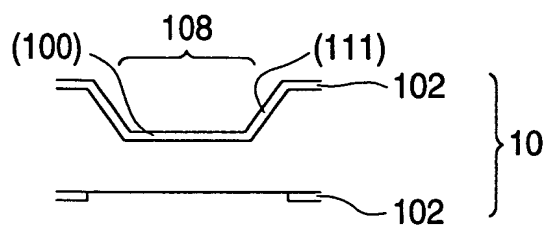


FIG. 4C

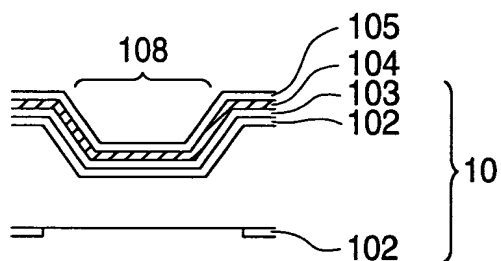


FIG. 4D

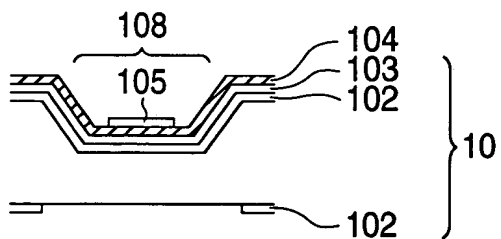


FIG. 4E

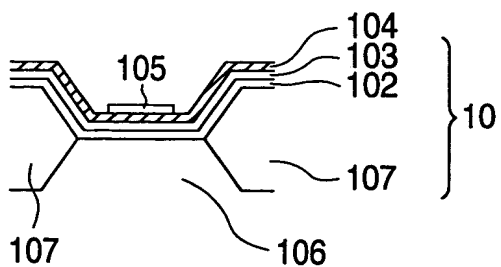


FIG. 5

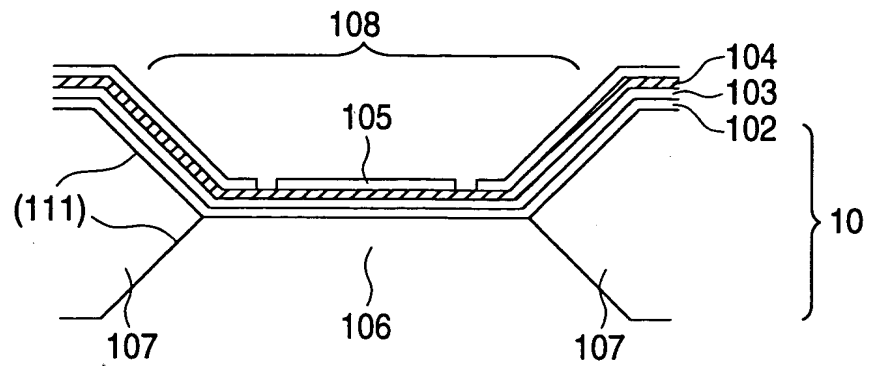


FIG. 6

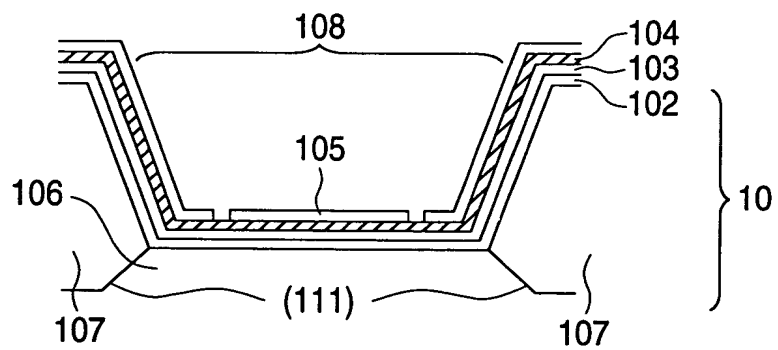


FIG. 7

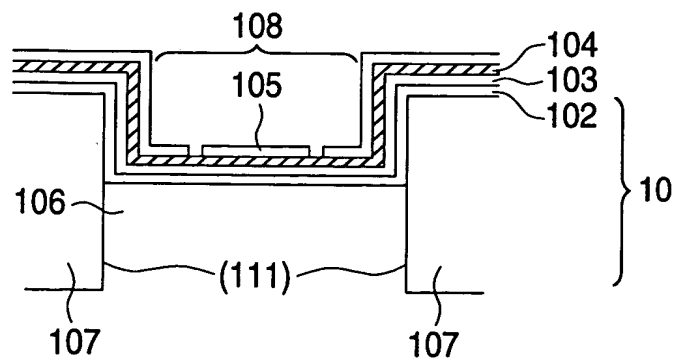


FIG. 8

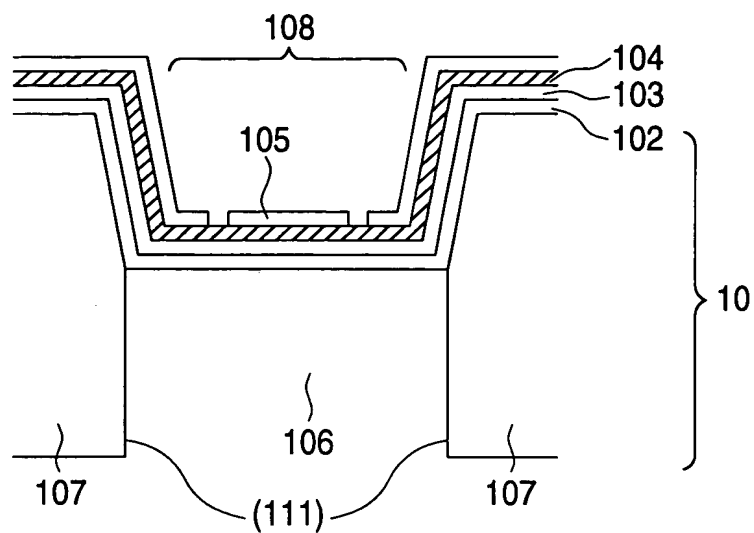
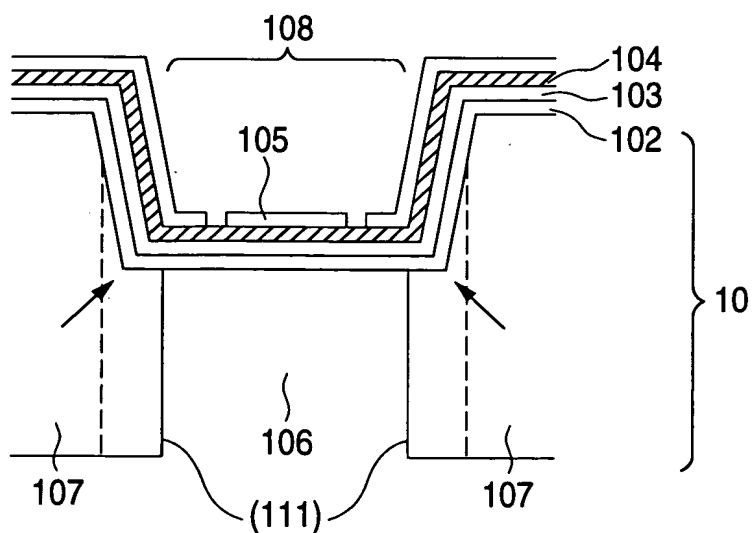
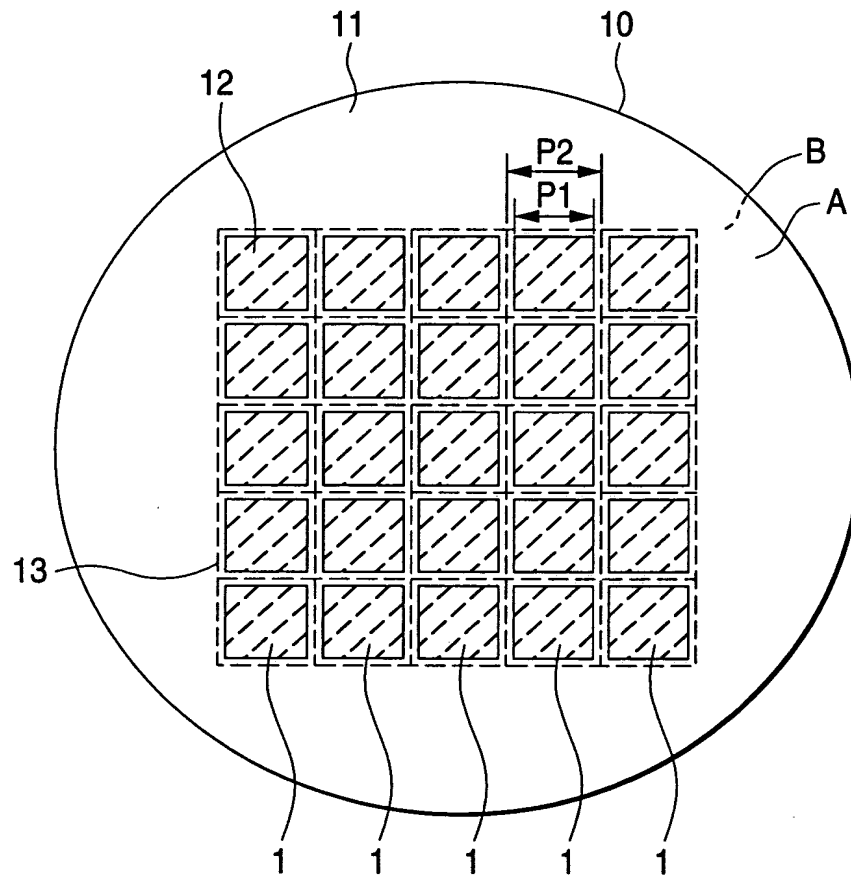


FIG. 9



**FIG. 10**



pressurizing  
chamber substrates

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FIG. 11

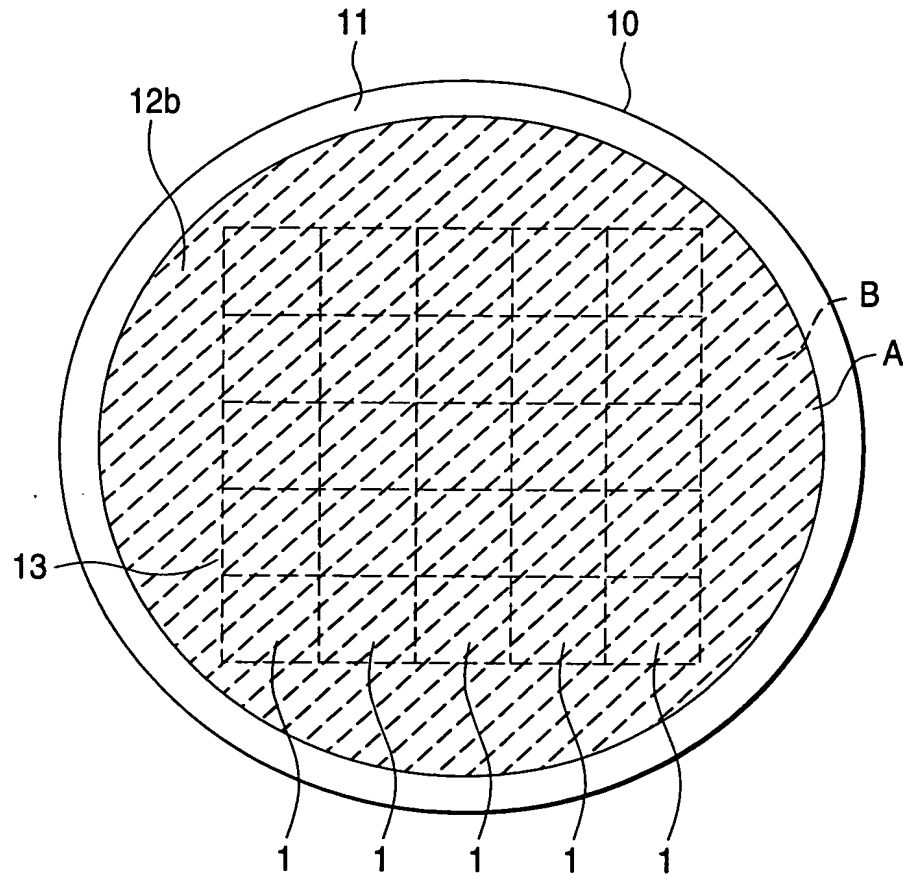




FIG. 12A

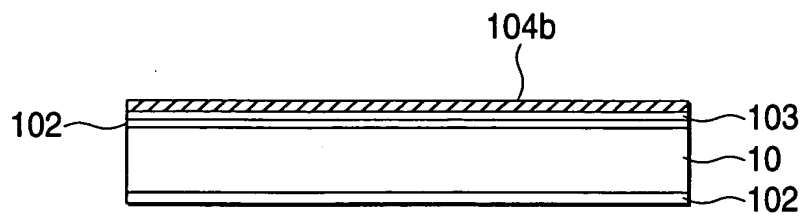


FIG. 12B

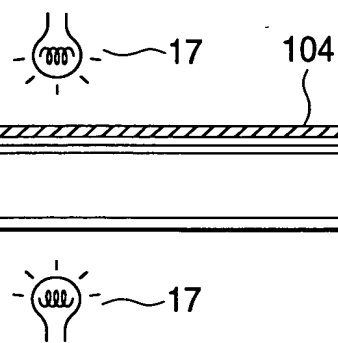


FIG. 12C

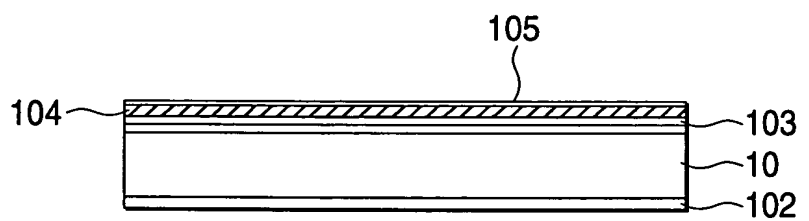


FIG. 12D

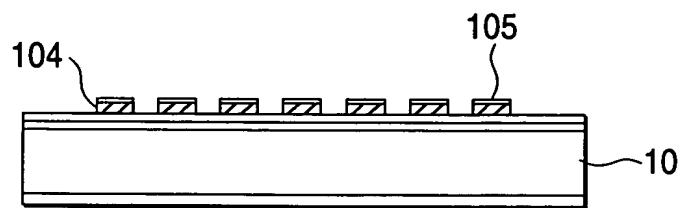
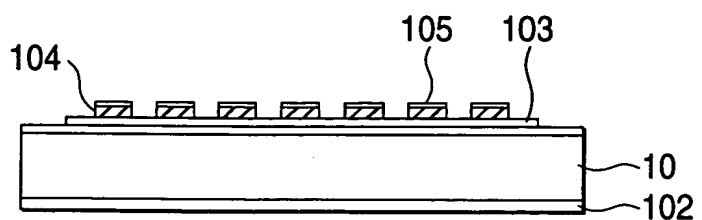


FIG. 12E



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FIG. 13F

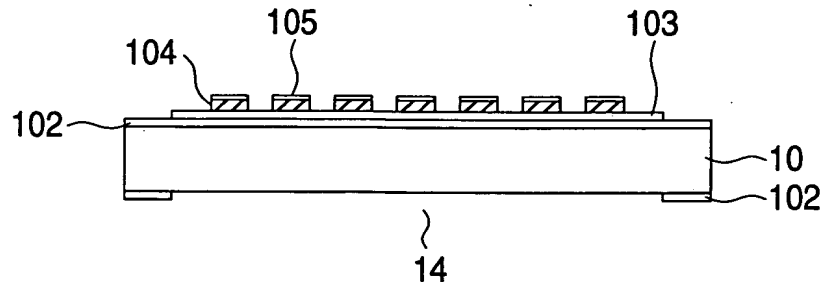


FIG. 13G

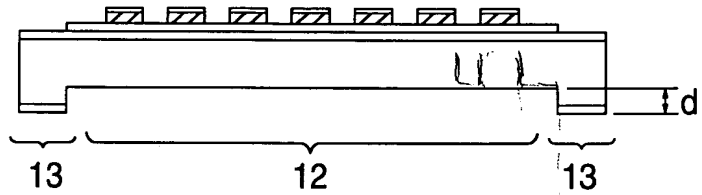


FIG. 13H

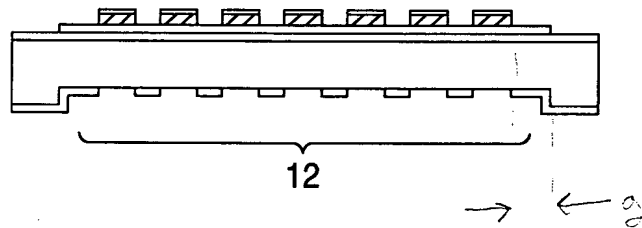


FIG. 13I

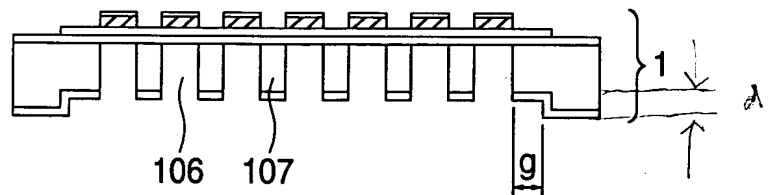
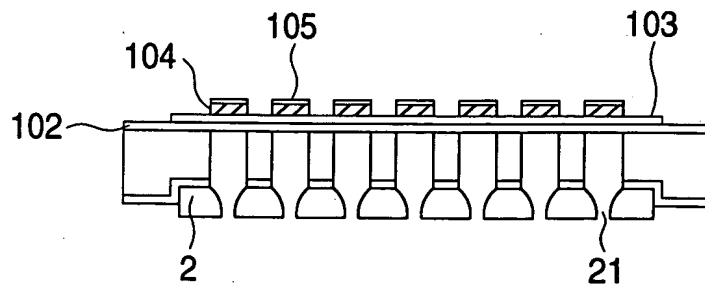


FIG. 13J



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FIG. 14

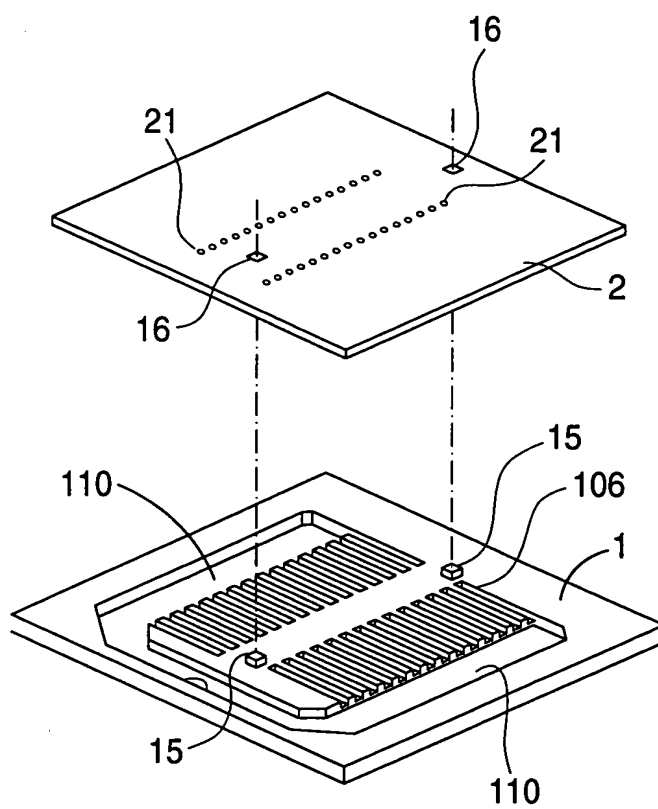


FIG. 15F

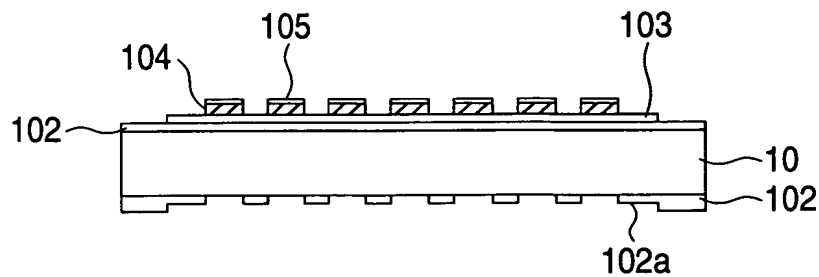


FIG. 15G

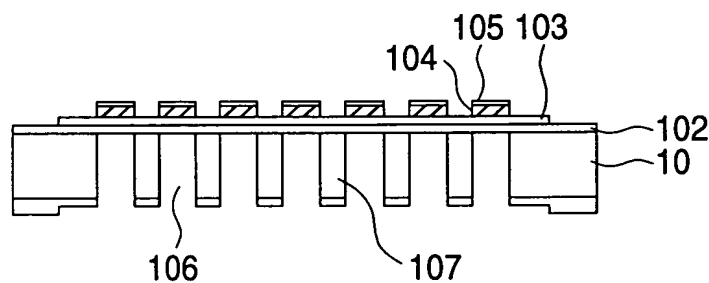


FIG. 15H

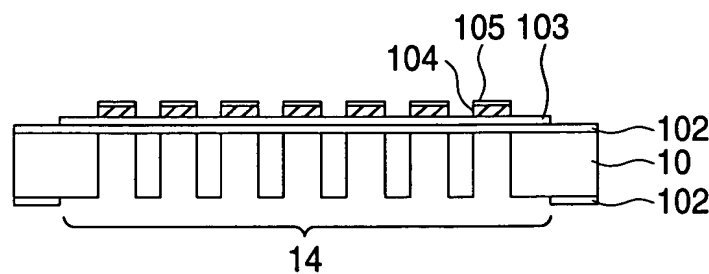
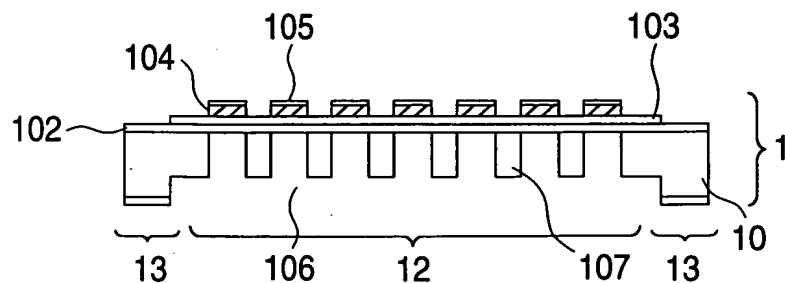


FIG. 15I



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FIG. 16

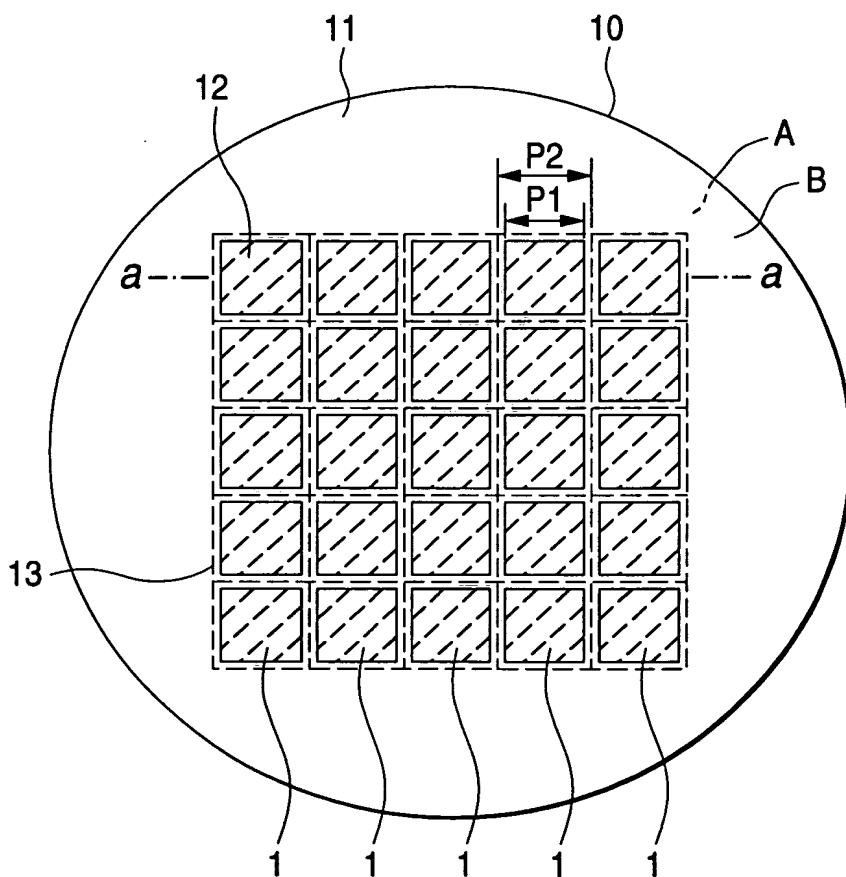


FIG. 17A

WATER CLEANING



FIG. 17B

LAYER-TO-BE-PROCESSED  
FORMATION

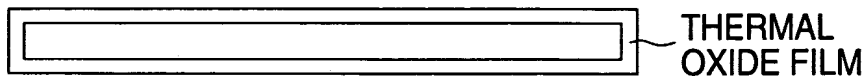


FIG. 17C

RESIST APPLICATION

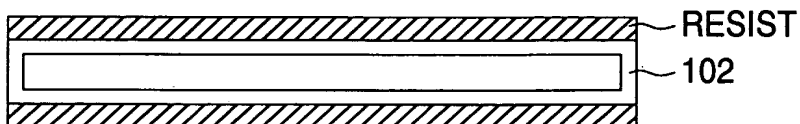


FIG. 17D

EXPOSURE

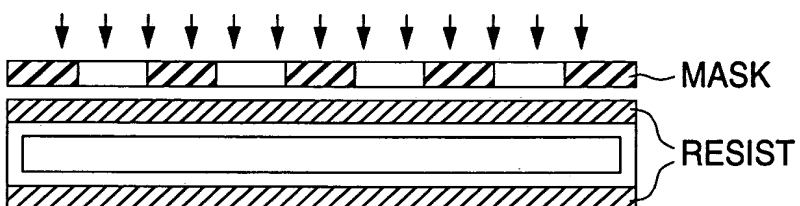


FIG. 17E

DEVELOPMENT

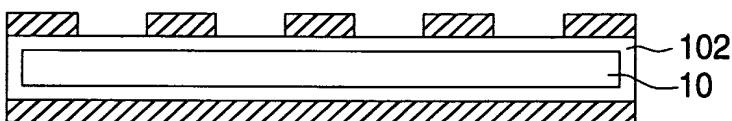


FIG. 17F

ETCHING

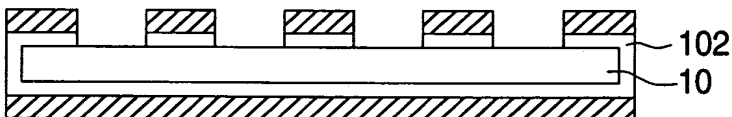


FIG. 17G

RESIST REMOVAL

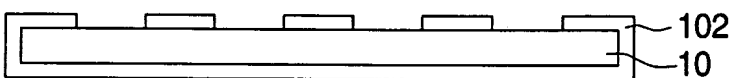


FIG. 17H

SILICON ETCHING

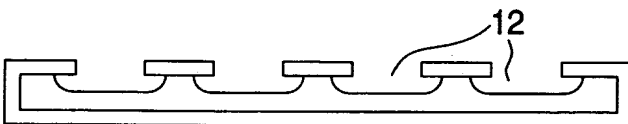


FIG. 17I

THERMAL OXIDE  
FILM ETCHING

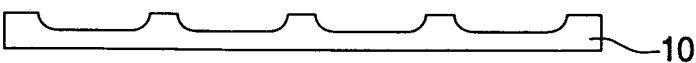


FIG. 17J

FILM-TO-BE-PROCESSED  
FORMATION

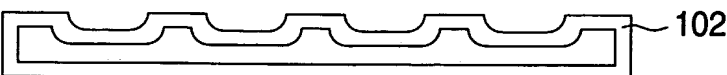


FIG. 18A

OSCILLATING PLACE  
FILM FORMATION

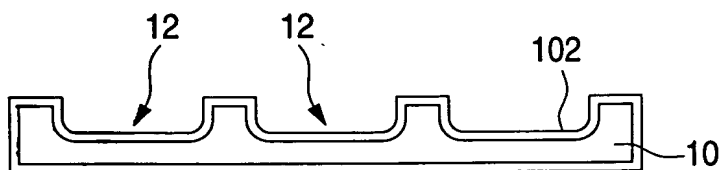


FIG. 18B

PIEZOELECTRIC  
SUBSTRANCE FORMATION

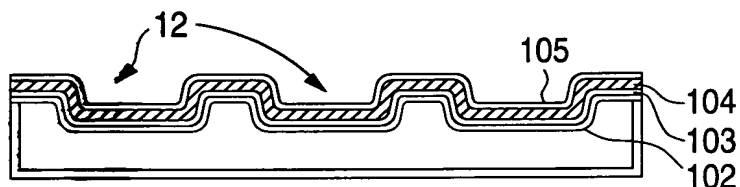


FIG. 18C

RESIST FORMATION

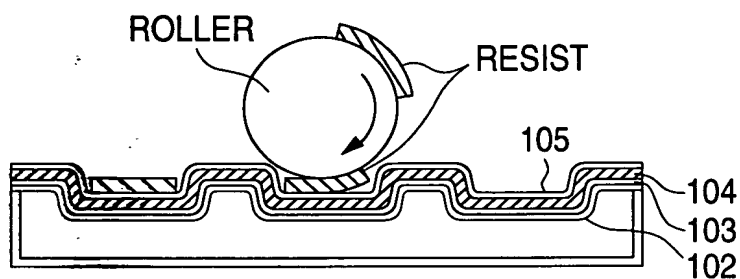


FIG. 18D

MASK EXPOSURE

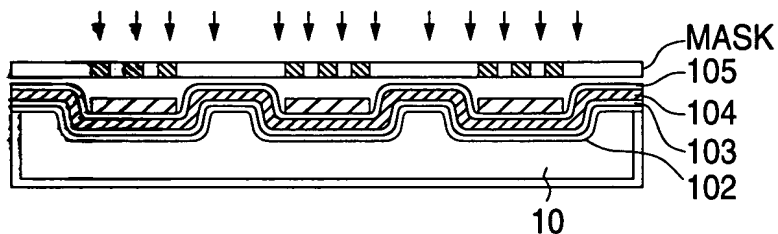


FIG. 18E

DEVELOPMENT

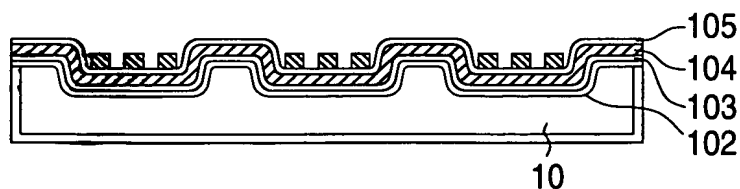
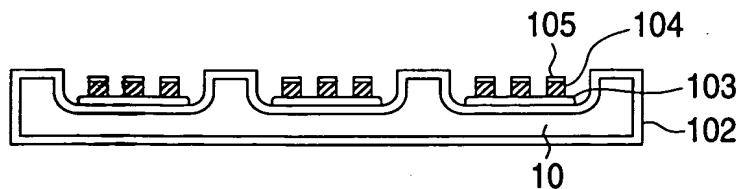


FIG. 18F

ETCHING



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FIG. 19

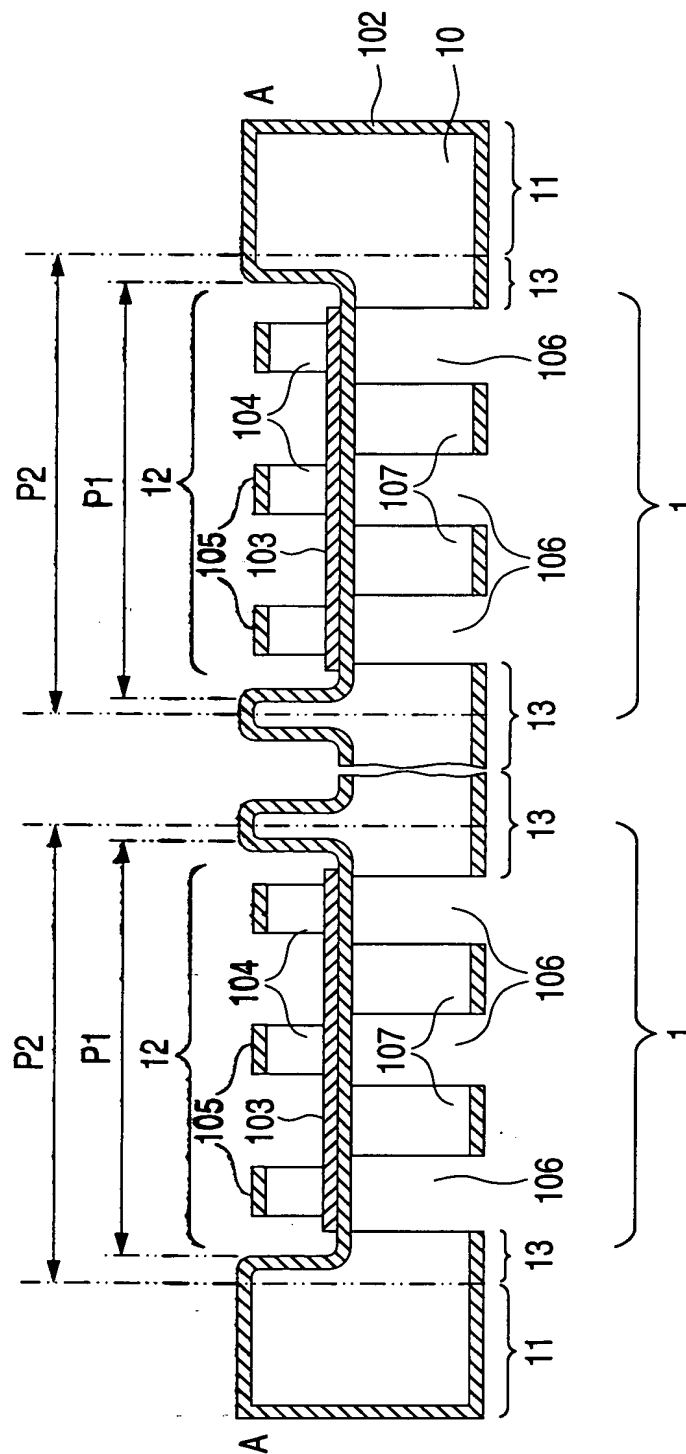




FIG. 20

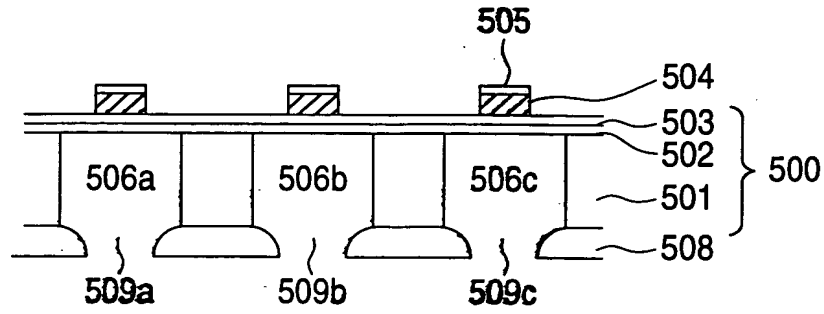


FIG. 21

